IN THE CLAIMS:

Please enter the following claim set:

1. (currently amended) A driver circuit comprising a semiconductor integrated circuit having a transistor in which a drive signal is applied to the transistor to drive the transistor to thereby drive a load, the driver circuit comprising:

an element region at least partially surrounded by an element isolation region;

a signal line that supplies the drive signal to the transistor, the signal line extending across the element region;

a gate dielectric layer formed in the element region;

a gate electrode layer, wherein part of the gate electrode layer is positioned on the gate dielectric layer in the element region and part of the gate electrode layer is positioned outside of the element region; ~~and~~

at least two connection sections that connect the signal line to the gate electrode layer, wherein at least one connection section is positioned outside of the element region and at least one connection section is positioned in the element region; and

wherein at least one connection section positioned in the element region includes a contact surface in direct contact with the gate electrode of the transistor, the transistor having a source region and a drain region, the contact surface including a center that is closer to the source region of the transistor than to the drain region of the transistor.

2. (currently amended) A driver circuit comprising a semiconductor integrated circuit having a plurality of transistors in which a single drive signal is applied to each of the transistors to drive the transistors to thereby drive a load, the driver circuit comprising:

an element region at least partially surrounded by an element isolation region;

a signal line for each of the transistors that supplies the drive signal and extends across the element region;

a gate dielectric layer on a semiconductor substrate in the element region for each of the transistors;

a gate electrode layer on the gate dielectric layer in the element region for each of the transistors, wherein part of the gate electrode layer extends to outside of the element region; and

at least two connection sections that connect the signal line to the gate electrode for at least one of the transistors, wherein a first connection section of the at least two connection sections is positioned outside of the element region and a second connection section of the at least two connections sections is positioned in the element region;

a source region and a drain region in the semiconductor substrate in the element region;

wherein the gate electrode layer is positioned over a portion of the semiconductor substrate that is located between the source region and the drain region;

wherein the gate electrode layer includes an upper surface including first and second upper surface areas that are positioned over the portion of the semiconductor substrate that is positioned between the source region and the drain region; and

wherein the first upper surface area is in direct contact with the second connection section, the second upper surface area is not in direct contact with the second connection section, and the second upper surface area is positioned closer to the drain region than to the source region.

3. (original) A driver circuit according to claim 2, wherein the at least two connection sections includes two or more connection sections provided for each of the transistors.

4. (original) A driver circuit according to claim 2, wherein the at least two connection sections includes two or more connection sections provided for each of the transistors except one of the transistors.

5. (original) A driver circuit according to claim 2, wherein at least two of the plurality of transistors have a different number of connection sections.

6. (original) A driver circuit according to claim 3, wherein at least two of the plurality of transistors have a different number of connection sections.

7. (original) A driver circuit according to claim 4, wherein at least two of the plurality of transistors have a different number of connection sections.

8. (original) A driver circuit according to claim 2, wherein the plurality of transistors have different numbers of connection sections.

9. (currently amended) A driver circuit comprising a semiconductor integrated circuit having a plurality of transistors in which a single drive signal is applied to each of the transistors to drive the transistors to thereby drive a load, the driver circuit comprising:

a signal line that supplies the drive signal, the signal line being separated from each of the transistors by a dielectric layer; and

connection sections for connecting the signal line to a gate electrode of each of the transistors, the connection sections being provided in a width direction of the gate electrode, wherein at least two of the plurality of transistors have a different number of connection sections;

wherein at least one connection section includes a contact surface in direct contact with the gate electrode of one of the transistors, the transistor having a source region and a drain region, the contact surface including a center that is closer to a source region of the transistor than to a drain region of the transistor.

10. (original) A driver circuit according to claim 9, wherein the plurality of transistors have different numbers of connection sections.

11. (canceled)

12. (currently amended) A driver circuit comprising a semiconductor integrated circuit having at least a first transistor in which a drive signal is applied to the first transistor, the driver circuit comprising:

an isolation region extending around an active region of a semiconductor substrate;

a gate dielectric layer on the active region;

a first gate electrode layer of the first transistor formed on the gate dielectric layer on the active region;

a first signal line that supplies the drive signal to the first transistor;

a first connection extending from the first signal line to the first gate electrode layer on the dielectric layer on the active region;

the first gate electrode layer also extending on the isolation region; and

a second connection extending from the signal line to the gate electrode layer on the isolation region.

wherein at least the first connection extending from the first signal line to the first gate electrode layer includes a contact surface in direct contact with the first gate electrode of the first transistor, the first transistor including a source region and a drain region, the contact surface including a center that is closer to the source region of the first transistor than to the drain region of the first transistor.

13. (previously presented) A driver circuit according to claim 12, wherein an additional dielectric layer is positioned between the signal line and the first gate electrode layer, and the at least two connections extend through the additional dielectric layer.

14. (previously presented) A driver circuit according to claim 13, wherein the first transistor includes source and drain regions positioned in the active region, and wherein a protective insulation layer is formed in direct contact with the first gate electrode and the source and drain regions.

15. (previously presented) A driver circuit according to claim 14, further comprising a silicide layer formed in direct contact with the source and drain regions.

16. (previously presented) A driver circuit according to claim 12 including a plurality of additional transistors, the driver circuit further comprising:

a gate electrode layer on a dielectric layer on the active region for each of the additional transistors;

a signal line for each of the additional transistors; and

at least one connection extending from the signal line for each of the additional transistors to the gate electrode layer on the dielectric layer on the active region for each of the additional transistors.

17. (previously presented) A driver circuit according to claim 16,

wherein the gate electrode layer for each of the additional transistors also extends on the isolation region; and

wherein at least one connection extends from the signal line for each of the additional transistors to the gate electrode layer on the isolation region.

18. (previously presented) A driver circuit according to claim 17, wherein at least two of the transistors have a different number of connections extending from the signal line to the gate electrode layer.

19. (currently amended) A driver circuit comprising a semiconductor integrated circuit having at least a first transistor in which a drive signal is applied to the first transistor, the driver circuit comprising:

an isolation region extending around an active region of the semiconductor substrate, the first transistor including source and drain regions formed in the active region;

a dielectric layer formed on the substrate;

a first gate electrode layer of the first transistor formed on the dielectric layer on the semiconductor substrate and extending across the active region;

a first signal line that supplies the drive signal, the first signal line extending across the active region; and

at least two connections extending from the first signal line to the first gate electrode, wherein at least one of the connections is positioned directly over the active region;

wherein at least one connection that is positioned over the active region includes a lower surface having a center that is closer to the source region than to the drain region.

20. (previously presented) A driver circuit as in claim 20, further comprising additional transistors, the driver circuit further comprising:

a gate electrode layer on a dielectric layer on the active region for each of the additional transistors;

a signal line for each of the additional transistors; and

at least one connection section extending from the signal line for each of the additional transistors to the gate electrode layer on the dielectric layer on the active region for each of the additional transistors.

21. (previously presented) A driver circuit according to claim 20, wherein at least two of the transistors have a different number of connections extending from the signal line to the gate electrode layer.

22. (new) A driver circuit comprising a semiconductor integrated circuit having a transistor in which a drive signal is applied to the transistor to drive the transistor to thereby drive a load, the driver circuit comprising:

a element region at least partially surrounded by an element isolation region;

a signal line that supplies the drive signal to the transistor, the signal line extending across the element region;

a gate dielectric layer formed in the element region;

a gate electrode layer, wherein part of the gate electrode layer is positioned on the dielectric layer in the element region and part of the gate electrode layer is positioned outside of the element region; and

at least two connection sections that connect the signal line to a gate electrode layer, wherein at least one connection section is positioned outside of the element region and at least one connection section is positioned in the element region; and

wherein the transistor includes a source region and a drain region, and the signal line includes a signal line portion positioned over part of the source region.

23. (new) A driver circuit as in claim 22, further comprising an interlayer dielectric layer positioned between the signal line portion and the part of the source region.

24. (new): A driver circuit comprising a semiconductor integrated circuit having a transistor in which a drive signal is applied to the transistor to drive the transistor to thereby drive a load, the driver circuit comprising:

a element region at least partially surrounded by an element isolation region;

a signal line that supplies the drive signal to the transistor, the signal line extending across the element region;

a first dielectric layer comprising a gate dielectric layer formed in the element region;

a gate electrode layer, wherein part of the gate electrode layer is positioned on the gate dielectric layer in the element region and part of the gate electrode layer is positioned outside of the element region; and

at least two connection sections that connect the signal line to a gate electrode layer, wherein at least one connection section is positioned outside of the element region and at least one connection section is positioned in the element region;

the transistor including a source region and a drain region in the element region; and

a second dielectric layer, wherein the signal line including a signal line portion that is separated from the source region by the second dielectric layer.

25. (new): A driver circuit as in claim 24, wherein the source region and the signal line portion are positioned so that a line extending perpendicular from an upper surface of part of the source region will contact the signal line portion.

Remarks

A Request for Continued Examination and an Information Disclosure Statement were filed for this application on August 4, 2003. In this Amendment, claims 1-2, 9, 12 and 19 have been amended and new claims 22-25 have been added. Claim 11 was previously canceled. Claims 1-10 and 12-25 are currently pending. Reexamination and reconsideration are respectfully requested.

New claims 22-21 have been added. Support for these claims may be found throughout the specification and figures. It is believed that no new matter has been entered. Examination is respectfully requested.

Applicant also notes that the record does not indicate than an IDS mailed to the Patent Office on April 12, 2003 was reviewed by the Examiner. Applicant also notes that an IDS was mailed on August 4, 2003 with the RCE papers. Applicant respectfully requests that the Examiner review and enter both of these IDS papers.

Applicant respectfully submits that the pending claims are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, or if the Examiner has any questions regarding this Amendment or the IDS papers, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes

Alan S. Raynes **August 22, 2003 (Date)**